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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,610	03/18/2004	Jonathan Doan	P119-US	9506

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REFLECTIVITY, INC.
350 POTRERO AVENUE
SUNNYVALE, CA 94085

EXAMINER	
GEORGE, PATRICIA ANN	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,610	DOAN ET AL.	
	Examiner	Art Unit	
	Patricia A. George	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,14,16,19-57 and 62* is/are rejected.

7)☒ Claim(s) *1,12,13,15,18,20,21,34,38,39,41,43-47 and 58-61* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-18-04, 10-27-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1 objected to because of the following informalities: The term "the microstructure" is referring to a structure not yet referenced. Please consider changing the term "the" to - - - a - - - . Appropriate correction is required.

Claims 20, 21, 46, and 47 are objected to because of the following informalities: The term "the" is specific, when the reference material is generic. Please consider changing the term "the" to - - - an - - - . Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 34, 43, and 44-48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 34, 43, and 44 recites the limitation "first area" in line one of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claims 45, 46, 47, and 48 recites the limitation "second area" in line one of the claim. There is insufficient antecedent basis for this limitation in the claim.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claims 1, 2, 9, 10, 16, 17, 19, 27, 28, 30, 34, 35, 42, 45, 53, 54, 55, 56, 61, and 62 are provisionally rejected on the ground of nonstatutory double patenting over claims 1, 5, 14, 22, 23, 25, 41, 62, 63, 84, and 112 of copending Application No. 10/104,109; and claims 1, 2, 8, 17-19, 22- 23, 25-28, 32, 34, 42, 44-45, 48-49, 51-56, and 61 are provisionally rejected on the ground of nonstatutory double patenting over claims 1, 14-15, 25, and 41 of copending Application No. 10/270,465.

These are provisional double patenting rejections since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: The broad limitations of

applicants' independent claims either etch a work piece, as in claims1 and 27, or make a microstructure, as in claim 53. Whereas, claims 1-176 of copending Application No. 10/104,109 etch a sample of silicon; and claims 1-65 of copending Application No. 10/270,465 form an integrated circuit. As a result, the limitations of applicants' claims are much broader and fully encompass the limitations of the conflicting claims.

Claims 1, 2, 9-10, 11-19, 26-28, 30, 32-36, 42-45, 49, 50, 52-53, and 61 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 2-4, 6-7, 9-10, 17, 19, 21, 23, 27-28, 31-50, 54 of U.S. Patent No. 6,849,471; and claims 1, 2, 4-8, 10, 16-17, 27-28, 30-36, 42-45, 48-50, 52-53, and 61-62 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 2-24, 27, 29-38, and 47-53 of U.S. Patent No. 6,913,942.

Although the conflicting claims are not identical, they are not patentably distinct from each other because applicants' independent claims 1, 27, and 53, of the instant invention are broader than the limitations of the conflicting claims. The broad limitations of applicants' independent claims either etch a work piece, as in claims1 and 27, or make a microstructure, as in claim 53. Whereas, claims 1-63 of U.S. Patent No. 6,849,471 form a micro-electro-mechanical device; and claims 1-53 of U.S. Patent No. 6,913,942 form a micro-mirror device. As a result, the limitations of applicants' claims are much broader and fully encompass the limitations of the conflicting claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1, 10, 11, 14, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Fernandes et al. in US 5,310,626 evedenced by Leonard et al. in US 5506171.

As for claim 1, Fernandes et al. teaches a method of vapor phase etching (col. 4, line 55-56), which is written on being loaded into a vapor phase etcher where wafers are etched in a sealed etch chamber (evidenced by L Leonard et al. in US 5506171, see col.4, lines 30-35), where a first area (fig. 1, 16a) is removed (see fig. 2) and a second area remain (fig. 2, 14), and the second area (fig. 2, 14) comprises an intermetallic compound (see col. 3, lines 34-44).

As for claim 10, Fernandes et al. teaches a method of etching that is applied to mechanical devices such as micromachines (col. 8, lines 29-30).

As for claims 11 and 14, Fernandes et al. teaches the chemical etchant comprises HF.

As for claim 16, Fenandes anticipates the substrate is made of silicon (col. 3, lines 26-28).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2-9, 17, 19-37, 40, 42-43, and 45-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fernandes et al. in US 5,310,626.

As for claims 2-7, Fernandes et al. teaches an effective method of etching which includes an intermetalic layer (part 14 of fig. 2) that may be a plurality of oxides or metal layers or active or inactive device layers, however Fernandes et al. does not identify the specific materials as claimed by applicants.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to etch the specific materials as applicants' limitations in claims 2-7, because Fernandes et al. teaches the method of etch is known to be effective when

performed at any level within any integrated circuit (col. 3, lines 40-44). Since, the references of Fernandes does not limit the materials etched, one of ordinary skill would etch any material present in the desired layer to be etched, including applicants specifically claimed compounds.

As for claim 8, Fernandes et al. teaches the first area is one of a conformal inorganic material, inorganic dielectrics, or nitride materials. Fernandes et al. does not specifically name the nitride materials as applicants' limitations in claim 8. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made, to select an elemental metal, metalloid, metal alloy, metal silicide, WxN, or TaN material for the first area, because Fernandes et al. teaches any inorganic material can be selected, and all the materials applicants' claim are known to be conformal inorganic materials.

As for claim 9, Fernandes et al. teaches a method of etching that is applied to mechanical devices such as micro-machines (col. 8, lines 29-30). However, Fernandes et al. does not specifically name micro-mirror arrays as in applicant's limitation.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to apply Fernandes' method of etching to micro-mirror arrays as in applicant's limitation, because the reference does not limit the type of mechanical devices etched. In the absence of unexpected results, it would have been obvious to etch any desired mechanical device, including applicants' specifically claimed micro-mirror array.

As for claim 17, Fernandes et al. further teaches (see figure 15) a barrier layer (part 32 and col. 7, lines 18-34) disposed between the structural layer (fig. 15, part 14) and the first area (fig 15., part 16a); and the first area is one of a conformal inorganic material.

Fernandes et al. does not specifically name amorphous silicon as applicants' limitations in claim 17. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made, to select polysilicon as an inorganic amorphous silicon for the first area, because Fernandes et al., because Fernandes et al. teaches the method of etch is known to be effective when performed at any level within any integrated circuit (col. 3, lines 40-44). In the absence of unexpected results, one of ordinary skill would remove any material present in first area to be etched, including applicants' specifically claimed amorphous silicon, because the reference does not limit the material etched.

As for claims 19-25, Fernandes et al. teaches an effective method of etching which includes an intermetallic layer (part 14 of fig. 2) that may be a plurality of any semiconductive layers, however Fernandes et al. does not identify the specific materials as claimed by applicants.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to select the specific materials as applicants' limitations in claims 19-25, because Fernandes et al. teaches the method of etch is known to be effective when performed at any semiconductive layer such as those claimed by applicants

within any integrated circuit (col. 3, lines 40-44). In the absence of unexpected results, one of ordinary skill would remove any material present in first area to be etched, including applicants' specifically claimed amorphous silicon, because the reference does not limit the material etched.

As for claim 26, see discussion toward claim 17, above.

As for claims 27 and 42, Fernandes et al. teaches a silicon substrate is provided (see fig. 2 and col.3. lines 26-30), figure 15, shows layers 16 a and 34 have been deposited as sacrificial layers on the substrate, a formed structural layer 14 which consists of multiple layers, and the removal of at least portions of the sacrificial layers is shown in figure 16.

Fernandes et al. teaches device layer 14 may be a plurality layers, however Fernandes et al. does not identify first and second structural layers within device layer 14, of figure 15.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to identify first and second structural layers as in applicants claim, when identifying a device layer because Fernandes et al. teaches the device layer consists of stacked layers.

Although Fernandes et al. teaches the sacrificial layer is an inorganic, Fernandes et al.does not specifically name a intermetallic material. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made, to etch an intermetalic material (different from the conductive material of the structural layer) as the

sacrificial layer. Since, the references of Fernandes does not limit the materials etched, one of ordinary skill would etch any material present in the desired layer to be etched, including applicants specifically claimed compounds.

As for claim 28 – 33, see the discussion toward claims 2-7 above.

As for claim 34, see the discussion toward claim 8 above.

As for claim 35, see the discussion toward claim 9 above.

As for claim 36, see the discussion toward claim 10 above.

As for claims 37 and 40, see the discussion toward claims 11 and 14 above.

As for claim 43, see the discussion toward claim 17 above.

As for claims 45 – 51, see the discussion toward claims 19-25 above.

As for claim 52, see discussion toward claim 26 above.

As for claim 53, Fernandes et al. teaches a method of forming semiconductor (i.e. microstructure), see Field of Invention, depositing a structural layer (fig. 15 & 16, part 36b), after the sacrificial layer (parts 16a) and the structural layer comprises a conductive material, and the sacrificial layer comprises an inorganic material.

Although Fernandes et al. teaches the sacrificial layer is an inorganic, Fernandes et al.does not specifically name a intermetallic material, however, it would have been obvious to one of ordinary skill in the art at the time of invention was made, to select an intermetalic material (different from the conductive material of the structural layer) for the sacrificial layer, because Fernandes et al. teaches any inorganic material can be selected, and intermetallic materials are inorganic materials.

As for claims 54-56, Fernandes et al. teaches an effective method of etching which includes an intermetalic layer (part 14 of fig. 2) that may be a plurality of oxides or metal layers or active or inactive device layers, however Fernandes et al. does not identify the specific materials as claimed by applicants.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to select the specific materials as applicants' limitations in claims 2-7, because Fernandes et al. teaches the method of etch is known to be effective when performed at any level within any integrated circuit (col. 3, lines 40-44). In the absence of unexpected results, one of ordinary skill would remove any material present in first area to be etched, including applicants' specifically claimed amorphous silicon, because the reference does not limit the material etched.

As for claim 57, see discussion toward claim 11 above.

Indication of Allowable Subject Matter

Claims 12, 13, 15, 18, 38, 39, 41, 44, and 58-62 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

The following is a statement of reasons for the indication of allowable subject matter:

As for claims 12, 38, and 58; 13, 39, and 59; 15, 41, and 60, search of prior art of record does not disclose use of bromine trifluorine; xenon difluorine; or a diluent gas that is a noble gas when spontaneously vapor phase etching a second area comprising inter-metallic compound.

As for claims 18 and 44, search of prior art of record does not disclose spontaneously vapor phase etching a second area comprising inter-metallic compound when the first area comprises amorphous silicon; the microstructure further comprises a structural layer and a barrier layer disposed between the first area and structural layer; and the removal of the barrier layer.

As for claims 61, search of prior art of record does not disclose use of xenon difluorine when spontaneously vapor phase etching a second area comprising inter-metallic compound of an early transitional metal.

As for claims 62, search of prior art of record does not disclose use of xenon difluorine when spontaneously vapor phase etching a second area comprising inter-metallic compound of an early transitional metal that is a sputtered elemental material.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571)272-5955. The examiner can normally be reached on weekdays between 7:00am and 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571)272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Patricia A George
Examiner
Art Unit 1765

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER